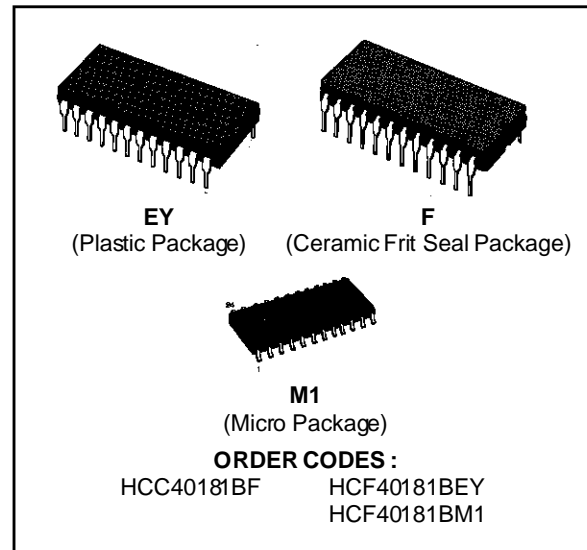


4-BIT ARITHMETIC LOGIC UNIT

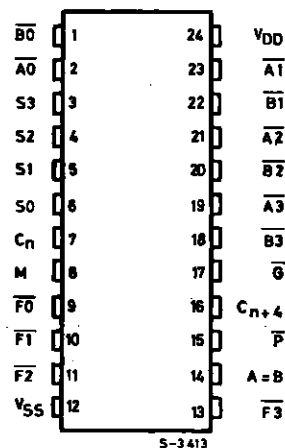
- FULL LOOK-AHEAD CARRY FOR SPEED OPERATIONS ON LONG WORDS
- GENERATES 16 LOGIC FUNCTIONS OF TWO BOOLEAN VARIABLES
- GENERATES 16 ARITHMETIC FUNCTIONS OF TWO 4-BIT BINARY WORDS
- A = B COMPARATOR OUTPUT AVAILABLE
- RIPPLE-CARRY INPUT AND OUTPUT AVAILABLE
- TYPICAL ADDITION TIME 200ns @ $V_{DD} = 10V$
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

DESCRIPTION

The **HCC40181B** (extended temperature range) and **HCF40181B** (intermediate temperature range) are monolithic integrated circuits, available in 24-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF40181B** is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive-OR and-NOR in the logical mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The **HCC/HCF40181B** operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table. The **HCC/HCF40181B** contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs \bar{G} and



PIN CONNECTIONS



HCC/HCF40181B

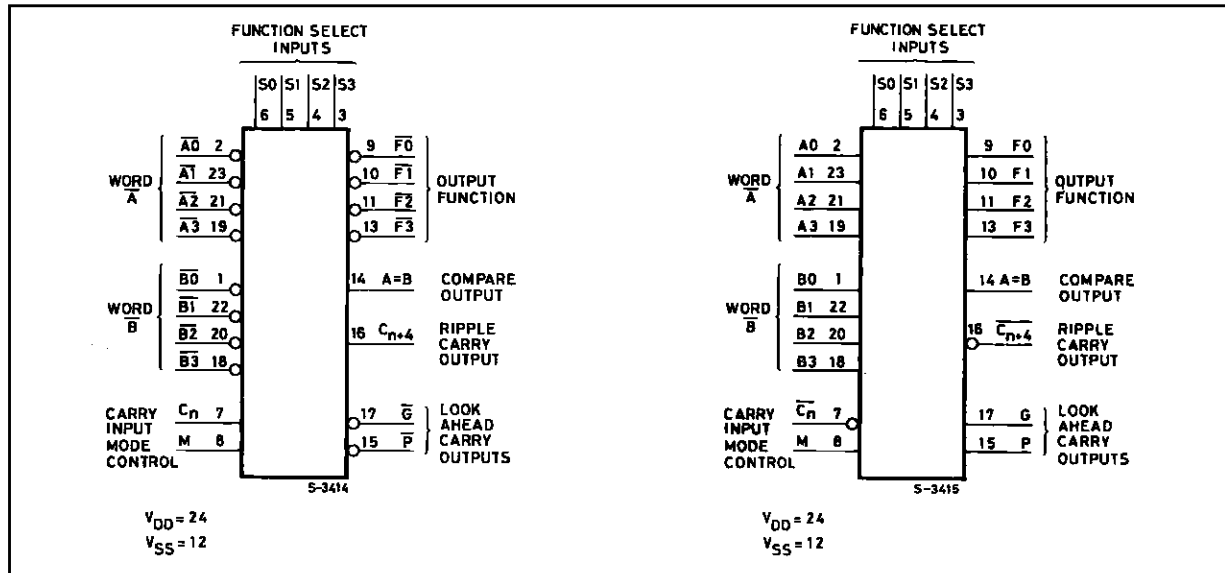
\bar{P} for the four bits of the **HCC/HCF40181B**. Use of the **HCC/HCF40182B** look-ahead carry generator in conjunction with multiple **HCC/HCF40181B**'s permits high-speed arithmetic operations on long words. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance. Also included in the **HCC/HCF40181B** is a comparator output $A = B$, which assumes a high

level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the subtract mode and externally decoding using the information in table II. The **HCC/HCF40181B** is similar to industry types MC 14581 and 74181.

FUNCTIONAL DIAGRAM

Active-low Data.

Active-high Data.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}^*	Supply Voltage : HCC Types HCF Types	- 0.5 to + 20 - 0.5 to + 18	V
V_i	Input Voltage	- 0.5 to $V_{DD} + 0.5$	V
I_i	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for $T_{op} =$ Full Package-temperature Range	200 100	mW
T_{op}	Operating Temperature : HCC Types HCF Types	- 55 to + 125 - 40 to + 85	$^{\circ}$ C
T_{stg}	Storage Temperature	- 65 to + 150	$^{\circ}$ C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to V_{SS} (GND).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage : HCC Types	3 to 18	V
	HCF Types	3 to 15	V
V _I	Input Voltage	0 to V _{DD}	V
T _{op}	Operating Temperature : HCC Types	- 55 to + 125	°C
	HCF Types	- 40 to + 85	°C

TRUTH TABLES

Table 1.

Function Select				Inputs/Outputs Active Low		Inputs/Outputs Active High	
				Logic Function (M=H)	Arithmetic* Function (M=L, C _n =L)	Logic Function (M=H)	Arithmetic* Function (M=L, C _n =H)
S3	S2	S1	S0				
0	0	0	0	\overline{A}	A minus 1	\overline{A}	A
0	0	0	1	\overline{AB}	AB minus 1	$\overline{A+B}$	A + B
0	0	1	0	$\overline{A+B}$	\overline{AB} minus 1	\overline{AB}	A + \overline{B}
0	0	1	1	Logic 1	minus 1	Logic 0	minus 1
0	1	0	0	$\overline{A+B}$	A plus (A + \overline{B})	\overline{AB}	A plus \overline{AB}
0	1	0	1	\overline{B}	AB plus (A + \overline{B})	\overline{B}	(A + B) plus \overline{AB}
0	1	1	0	$\overline{A \oplus B}$	A minus B minus 1	A \oplus B	A minus B minus 1
0	1	1	1	$\overline{A + \overline{B}}$	A + \overline{B}	\overline{AB}	\overline{AB} minus 1
1	0	0	0	\overline{AB}	A plus (A + B)	$\overline{A+B}$	A plus AB
1	0	0	1	A \oplus B	A plus B	$\overline{A \oplus B}$	A plus B
1	0	1	0	B	\overline{AB} plus (A + B)	B	(A + \overline{B}) plus AB
1	0	1	1	A + B	A + B	AB	AB minus 1
1	1	0	0	Logic 0	A plus A	Logic 1	A plus A
1	1	0	1	\overline{AB}	AB plus A	A + \overline{B}	(A + B) plus A
1	1	1	0	AB	\overline{AB} plus A	A + B	(A + \overline{B}) plus A
1	1	1	1	A	A	A	A minus 1

* Expressed as two's complement. For arithmetic function with C_n in the opposite state, the resulting function is as show plus 1.
 1 = HIGH LEVEL.
 0 = LOW LEVEL.

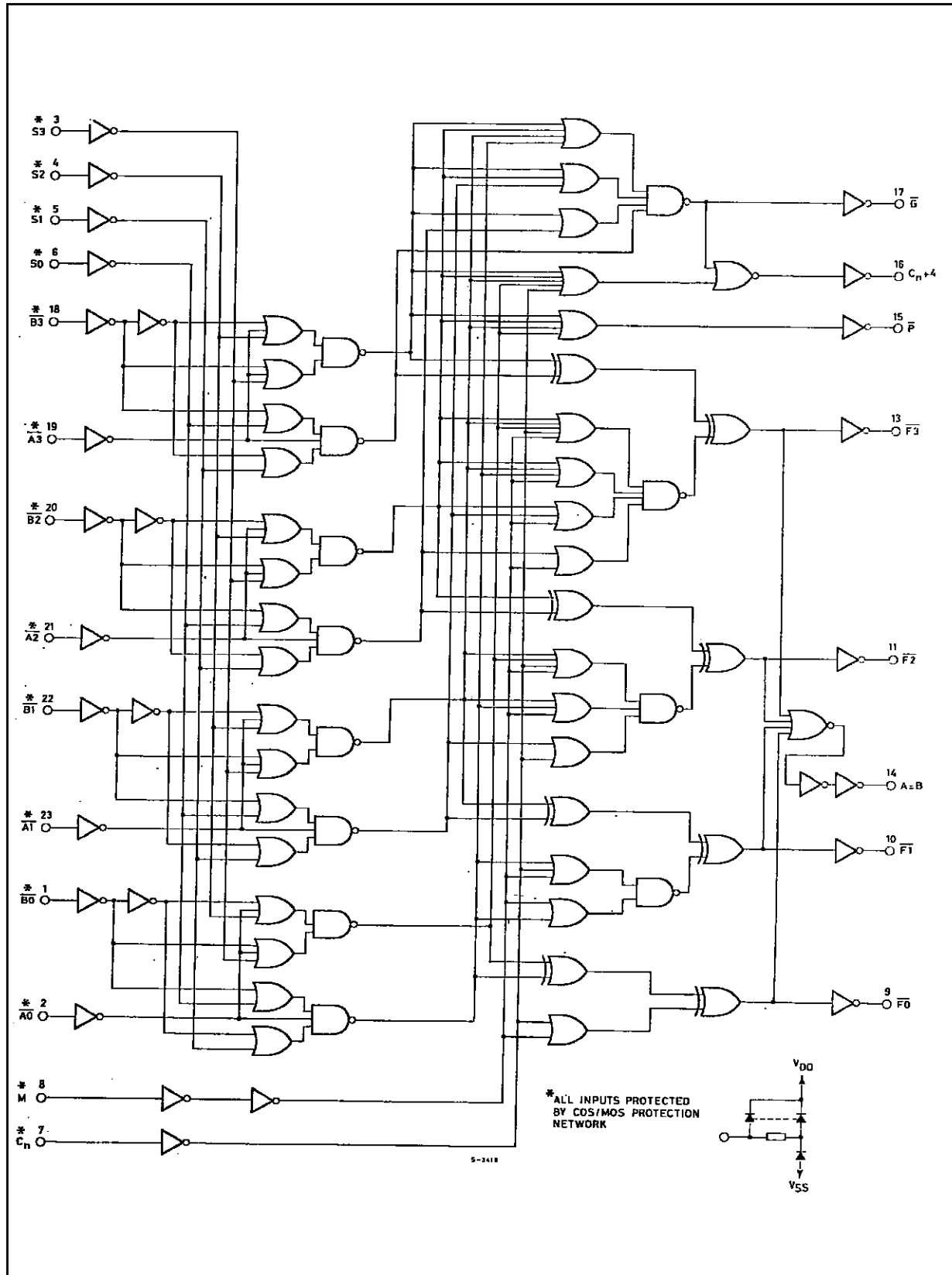
Table 2 : Magnitude Comparison.

Active-high Data			Active-low Data		
Input C _n	Output C _{n+4}	Magnitude	Input C _n	Output C _{n+4}	Magnitude
1	1	A ≤ B	0	0	A ≤ B
0	1	A < B	1	0	A < B
1	0	A > B	0	1	A > B
0	0	A ≥ B	1	1	A ≥ B

1 = HIGH LEVEL
 0 = LOW LEVEL

HCC/HCF40181B

LOGIC DIAGRAM Active-low Data



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value						Unit	
			V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{Low} *		25°C			T _{High} *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I _L	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	μ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
V _{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95		4.95		V	
			0/10		< 1	10	9.95		9.95		9.95			
			0/15		< 1	15	14.95		14.95		14.95			
V _{OL}	Output Low Voltage		5/0		< 1	5		0.05		0.05		0.05	V	
			10/0		< 1	10		0.05		0.05		0.05		
			15/0		< 1	15		0.05		0.05		0.05		
V _{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5		3.5		V	
				1/9	< 1	10	7		7		7			
				1.5/13.5	< 1	15	11		11		11			
V _{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5		1.5		1.5	V	
				9/1	< 1	10		3		3		3		
				13.5/1.5	< 1	15		4		4		4		
I _{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	- 2		- 1.6	- 3.2		- 1.15	mA	
			0/ 5	4.6		5	- 0.64		- 0.51	- 1		- 0.36		
			0/10	9.5		10	- 1.6		- 1.3	- 2.6		- 0.9		
			0/15	13.5		15	- 4.2		- 3.4	- 6.8		- 2.4		
		HCF Types	0/ 5	2.5		5	- 1.53		- 1.36	- 3.2		- 1.1		
			0/ 5	4.6		5	- 0.52		- 0.44	- 1		- 0.36		
I _{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL}	Input Leakage Current	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
		HCF Types	0/15	Any Input		15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C _I	Input Capacitance		Any Input						5	7.5			pF	

* T_{Low} = - 55°C for HCC device : - 40°C for HCF device.* T_{High} = + 125°C for HCC device : + 85°C for HCF device.The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.

HCC/HCF40181B

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$, typical temperature coefficient for all V_{DD} values is $0.3\%/^{\circ}\text{C}$, all input rise and fall time = 20ns)

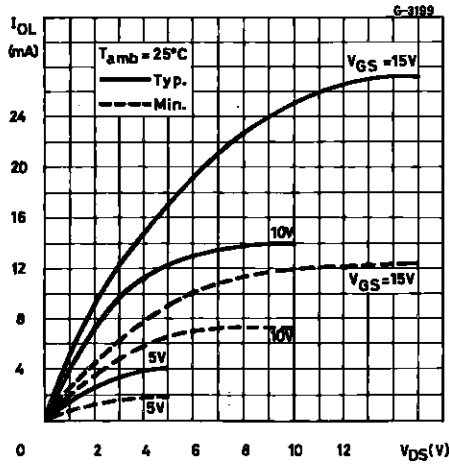
Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH} , t_{PHL}	Propagation Delay Time A or B to F (logic mode) A or B to G or P		5		400	800	ns
			10		160	320	
			15		120	240	
	A or B to F, C_{n+4} , or $A = B$		5		300	1000	ns
			10		200	400	
			15		140	280	
	C_n to F		5		320	640	ns
			10		135	270	
			15		100	200	
	C_n to C_{n+4}		5		200	400	ns
			10		100	200	
			15		70	140	
t_{TLH} , t_{THL}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	

Table 3 : AC Test Setup Reference (active-low data).

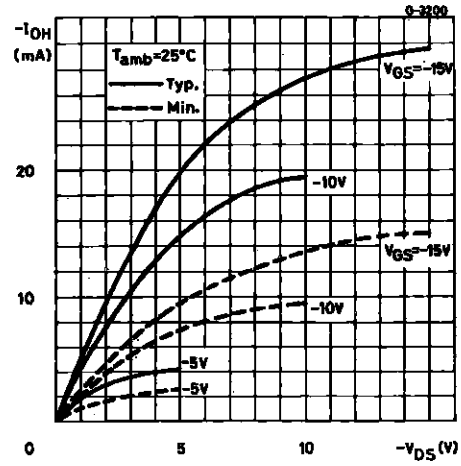
Test Delay Times	AC Paths		DC Data Inputs		Mode*
	Inputs	Outputs	to V_{SS}	to V_{DD}	
SUM_{IN} to SUM_{OUT}	\overline{BO}	Any \overline{F}	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, C_n	All \overline{A} 's	ADD
SUM_{IN} to P	\overline{AO}	\overline{P}	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, C_n	All \overline{B} 's	ADD
SUM_{IN} to \overline{G}	\overline{BO}	\overline{G}	All \overline{A} 's M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
SUM_{IN} to C_{n+4}	\overline{BO}	C_{n+4}	All \overline{A} 's, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
C_n to SUM_{OUT}	C_n	Any \overline{F}	All \overline{A} 's, M	All \overline{B} 's	ADD
C_n to C_{n+4}	C_n	C_{n+4}	All \overline{A} 's, M	All \overline{B} 's	ADD
SUM_{IN} to $A = B$	\overline{BO}	$A = B$	All \overline{A} 's $\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M	C_n	SUBTRACT
SUM_{IN} to SUM_{OUT} (logic mode)	All \overline{B} 's	Any \overline{F}	All \overline{A} 's, C_n	M	EXCLUSIVE OR

* ADD Mode : $S_0, S_3 = V_{DD}$; $S_1, S_2 = V_{SS}$. SUBTRACT Mode : $S_0, S_3 = V_{SS}$; $S_1, S_2 = V_{DD}$.

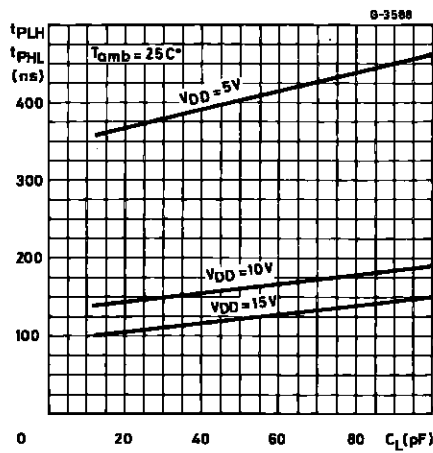
Output Low (sink) Current Characteristics.



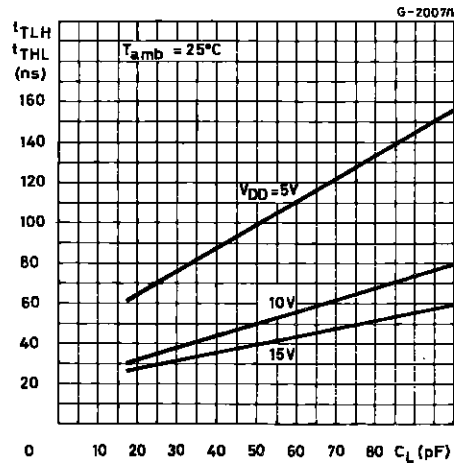
Output High (source) Current Characteristics.



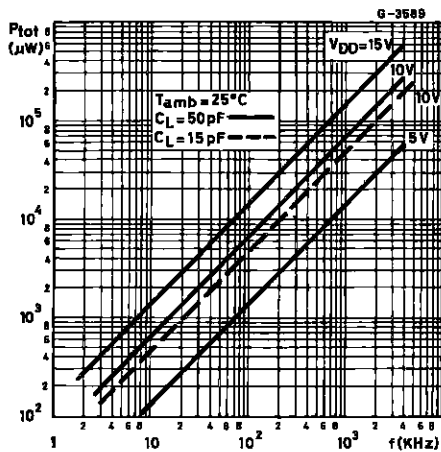
Typical Propagation Delay Time vs. Load Capacitance



(for A or B to F, logic mode).

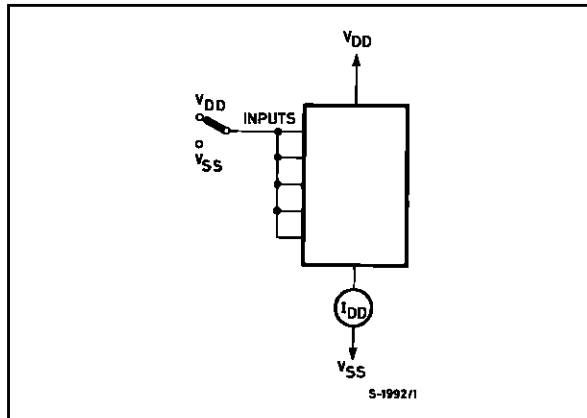


Typical Dynamic Power Dissipation vs. Input Frequency

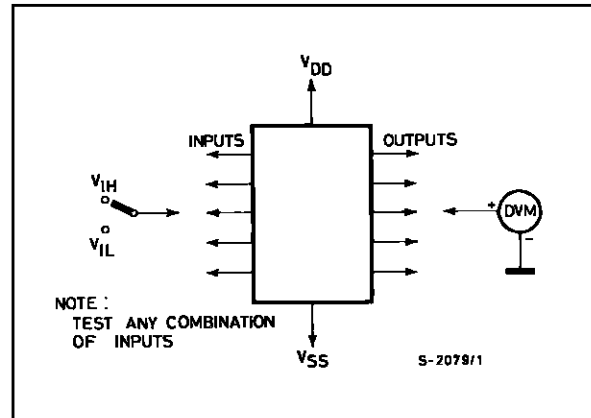


TEST CIRCUITS

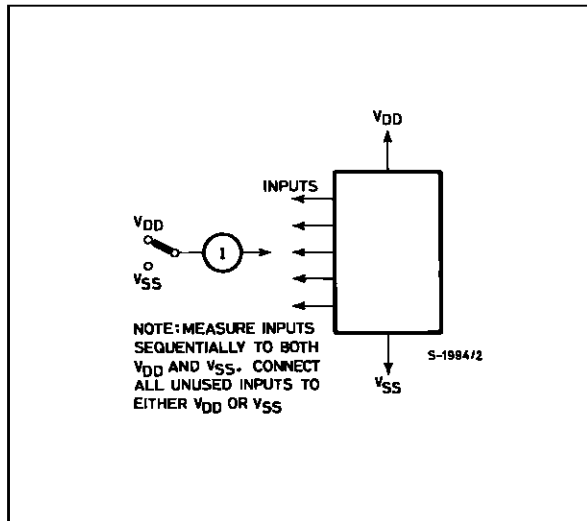
Quiescent Device Current



Input Voltage

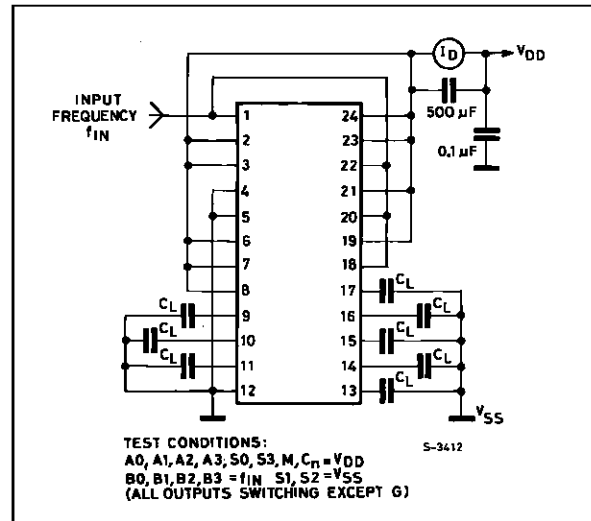


Input Leakage Current



NOTE: MEASURE INPUTS SEQUENTIALLY TO BOTH V_{DD} AND V_{SS} . CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

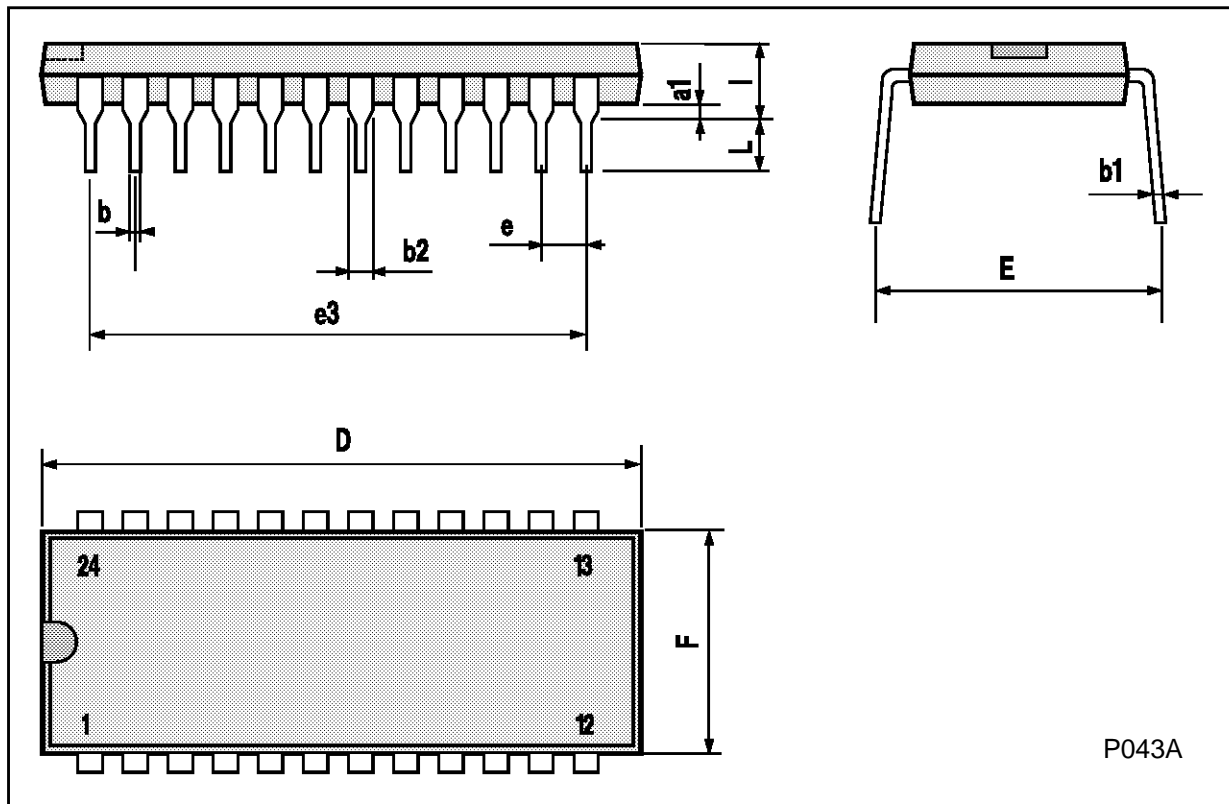
Dynamic Power Dissipation



TEST CONDITIONS:
 $A_0, A_1, A_2, A_3, S_0, S_3, M, C_n = V_{DD}$
 $B_0, B_1, B_2, B_3 = f_{IN}$ $S_1, S_2 = V_{SS}$
 (ALL OUTPUTS SWITCHING EXCEPT G)

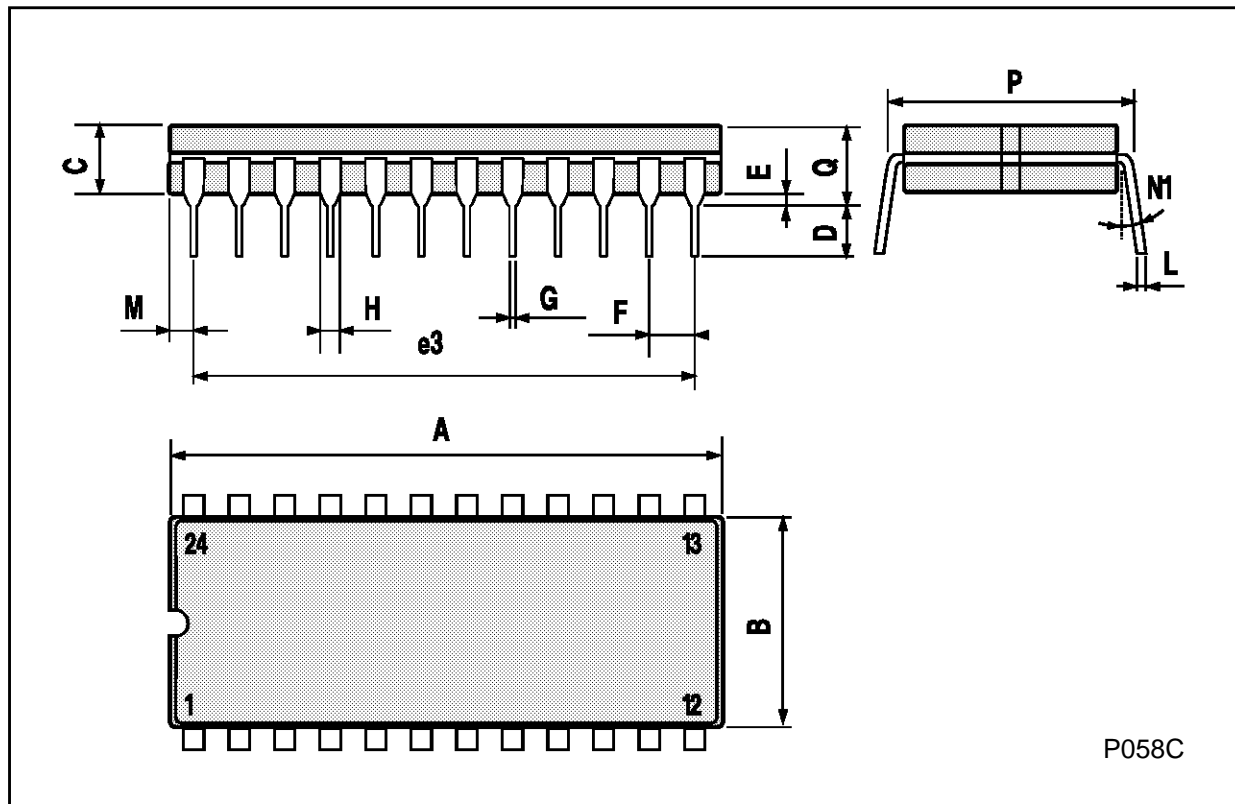
Plastic DIP24 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
l		4.445			0.175	
L		3.3			0.130	



Ceramic DIP24 MECHANICAL DATA

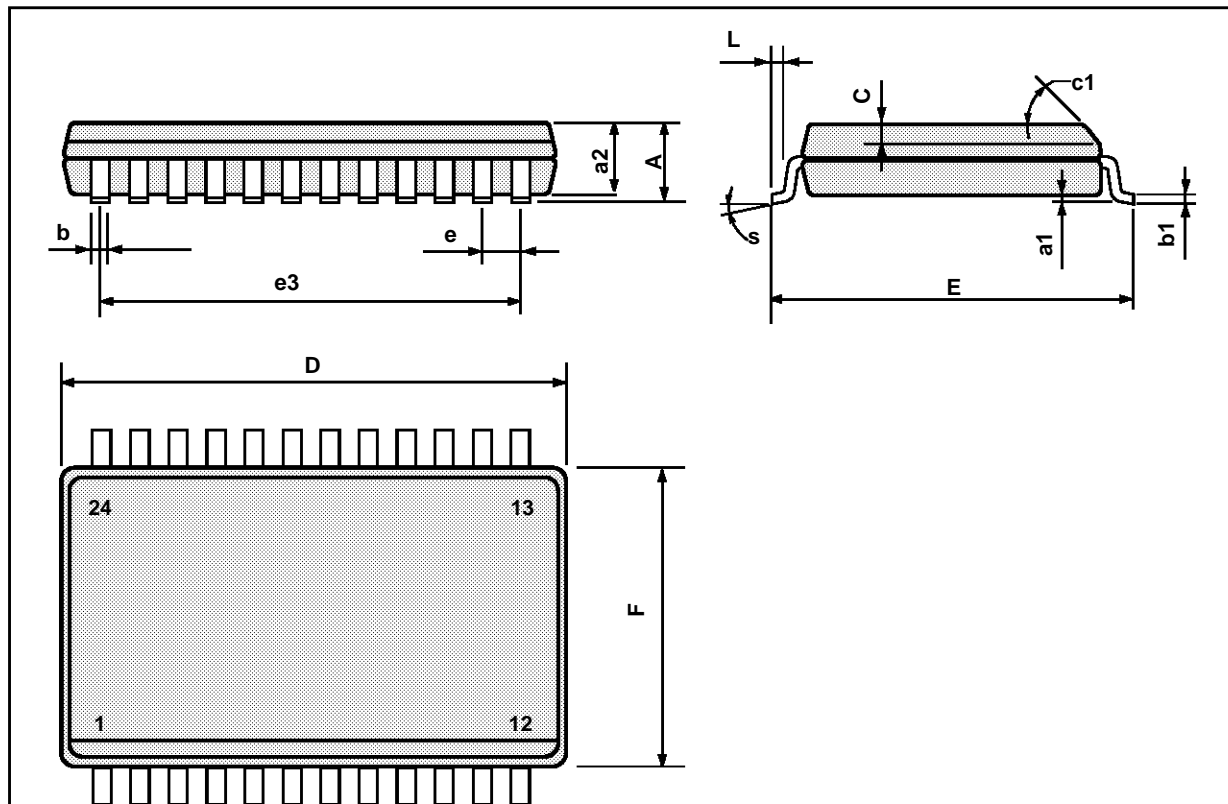
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			32.3			1.272
B	13.05		13.36	0.514		0.526
C	3.9		5.08	0.154		0.200
D	3			0.118		
E	0.5		1.78	0.020		0.070
e3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N1	4° (min.), 15° (max.)					
P	15.4		15.8	0.606		0.622
Q			5.71			0.225



P058C

SO24 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8° (max.)					



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